clk out

Figure 1

212 (X1)   214 (D2)

204

211   210(D1)   208

startup

216(C1)   202

D   D

Q   Q

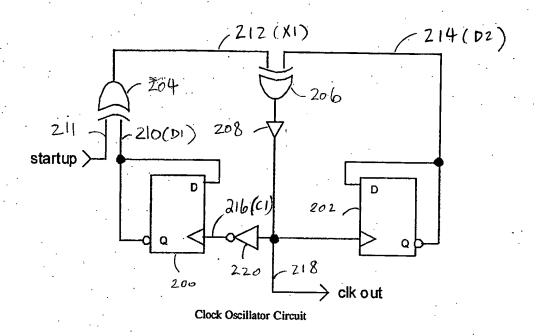200   220   218

clk out

Clock Oscillator Circuit

Figure 2

State	D1	Startup	X1	D2	Clkout	C1
0	1	1	0	0	0	1
1	1	0	1	0	1	0
2	1	0	1	1	0	1
3	0	0	0	1	1	0
4	0	0	0	0	0	1
5	1	0	1	0	1	0

Figure 3